Wafer Charging Bulletin Vol. 1, No. 2

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From the Editor ...

In this second issue of our bulletin, we present brief summaries of selected papers from the 1998 3rd International Symposium on Plasma Process-Induced Damage (P^2ID), and from the XIIth International Conference on Ion Implantation Technology (IIT'98).

While some papers present new findings obtained through the use of CHARM-2 charging monitors, others address the broader issues of charging damage to thin oxides, or compare results obtained with different charging monitors currently used in IC manufacturing.

Whenever appropriate, we quote directly from the original papers in order to retain the flavor of the original presentations. You may obtain copies of the complete papers from WCM.

Please note that in the future we plan to distribute this bulletin by e-mail. Since we may not have your e-mail address, please send it, along with yout company name, to **bulletin@charm-2.com.** Please mention this to your colleagues, as well.

New and exciting ...

- Prompted by the results Dr. M. E. Mack presented at IIT'98, we now provide log J vs. V plots of charging sources for purposes of measuring and monitoring plasma electron temperature (T_e). Non-uniformities in this important parameter have greater influence on charging potentials than non-uniformities in plasma density. We are amazed how readily these plots reveal changes in the operating characteristics of the charge control systems used in high current ion implanters.

- CHARM-2 results correlate to SPIDER damage. Detailed analysis of data first reported at IIT'98 shows that device physics should not be ignored when analyzing charging damage results, and tells us which charging parameters are really important with regard to charging damage in high current ion implanters. The details will be presented in future publications.

- CHARM-2 works really well in oxide deposition tools! Several unique CHARM-2 features, including the ability to work at temperatures above 400°C, the ability to separate UV effects from charging effects, and the ability to identify charging occurring at elevated temperature vs. at low temperature, provide unmatched ability to analyze and understand charging damage in plasma oxide deposition tools. CHARM-2 succeeded where the competition failed. The details will be presented in future publications.

IIT'98 paper summaries:

Monitoring Charging In High Current Ion Implanters Yields Optimum Preventive Maintenance Schedules And Procedures

(H. Gonzalez, et. al., Fairchild Semicond., West Jordan, UT)

In this paper, the authors describe the results of "using CHARM-2 to proactively monitor charging on a consistent basis over 12 months" to determine the causes of drift in negative charging on Eaton NV-10 high current implanters.

"A pattern was noticed where the negative charging levels changed, and was correlated to the monthly PM… Immediately after the monthly PM, low levels of negative charging (–0.9 to –14 volts) were recorded. The charging levels gradually increased from – 15 to –27 volts until the next monthly PM was performed."

"This trend prompted an investigation to determine what was influencing the change in negative charging potentials. One component of the monthly PM procedure was added to the weekly PM and performed for four weeks … This procedure was repeated for each component listed on the monthly PM until we determined what effect each component had on negative charging levels."

"The components included the flood gun, the extension tube, V3 assembly, sliding seals, wear plate insert, chamber, and disk… A key component that influenced and maintained a lower negative charging level …was the cleaning of the inside surface of the seal plate portion of the V3 isolation valve assembly." This component is now included in the new weekly PM procedure.

In summary, the authors conclude that "CHARM-2 is an effective real time in line monitor for preventing accidents that affect product quality."

Note: This is an excellent example of proactive problem avoidance, and yield optimization. (ed.)

Characterizing Electron Shower With CHARM-2 Wafers On Eaton NV-8200P Medium Current Ion Implanter

(S. Reno, et. al., Fairchild Semicond., West Jordan, UT)

In this paper, the authors characterized the charging performance of the Eaton NV-8200P medium current ion implanter using bare and patterned-resist covered CHARM-2 wafers. After determining that "the photoresist greatly enhanced positive charging", subsequent characterization used resist-covered CHARM-2 wafers to determine the optimum E-shower settings for different beam currents**.** Anomalous negative charging results with the E-shower OFF were also explained.

The authors conclude: "This paper shows that CHARM-2 wafers effectively characterize the charging environments of wafers during implant. By using the voltage and current sensors on CHARM-2, a complete picture of wafer charging is obtained. Also shown, an optimized E-Shower setting can increase yields at the higher beam currents."

Charge Control Performance of an Ultra-Low Energy Ion Implanter

(W. A. Krull, et. al., Motorola APRDL, Austin, TX)

Charging performance of Eaton NV-GSD/ULE ultra-low energy ion implanter was characterized using CHARM-2 and SEMATECH SPIDER. Excellent correlation was observed between SPIDER threshold voltage and transconductance shifts on n-channel and p-channel transistors, and CHARM-2 charging parameters.

Note: Detailed explanation of these results, taking into account n-channel and p-channel transistor device physics, and its influence on correlation (or lack of correlation) between SPIDER and CHARM-2 variables, will be presented in future publications. SEMATECH members can contact SEMATECH to obtain the latest results. At this time, we can only say that physics works, and that currents, not voltages, are the damage drivers – as explained in the first issue of our Wafer Charging Bulletin.

Optimized Charge Control for High Current Ion Implantation

(M. E. Mack, et. al., Eaton Corporation, Beverly, MA)

During a detailed explanation of the issues and remedies involved in developing an optimized plasma charge control system, M. Mack presented measurements of the plasma electron temperature (T_e) at the wafer surface (where it really counts!) using CHARM-2 wafers. The results were consistent with other Langmuir probe measurements described in the paper.

Note: Since then, WCM has implemented this function in its ChargeMap® equipment charging analysis reports.

Characterisation of a New Precision Implant 9200 Plasma Flood System

(E. H. J. Satink, et. al., Philips Semiconductors, The Netherlands)

In a poster presentation, E. Satink used CHARM-2 data to illustrate the superior performance of a new plasma charge control system for the Applied Materials Precision Implant 9200 high current ion implanter.

Photoresist Mask Design for Evaluation of Resist-Mediated Charging Effects During High Current Ion Implantation

(W. Lukaszek, et. al., WCM, Inc., Woodside, CA)

This paper describes the rationale behind a general approach to resist mask design, intended to emulate resist placement on CMOS product wafers. The approach was applied to the design of four-field reticles for use with the CHARM-2 monitors to provide a tool for optimization of implant conditions to minimize resist-mediated charging on product wafers. Both dark-field and light-field designs were described. The dark-field mask described in this paper was used in a comprehensive study of resist-mediated wafer charging described below.

Additional results presented in this paper indicate that light-field masks should be preferred for ion implants over dark-field masks, since they do not elevate positive potentials. Suppressing increased positive potentials with electron flood results in higher negative current densities for devices not under the beam. Since the negative current densities exhibit a long "tail" which can reach relatively high negative potentials, excessive electron flood can promote charging damage due to negative charging (evidence supporting this will be presented in future publications).

The difference in charging potentials between the dark-field and light-field masks obtained in these experiments also indicate that, depending on the polarity of the implant mask, different electron flood settings should be used for optimum charging performance.

Note: Both dark-field and light-field designs described in these papers can be obtained from Wafer Charging Monitors, Inc.

Photoresist Effects on Wafer Charging Control: Current-Voltage Characteristics Measured With CHARM-2 Monitors During High-Current As+ Implantation

(M. Current, et. al., Applied Materials, Santa Clara, CA)

The effects of ion energy, accumulated dose, photoresist coverage and patterning were studied using CHARM-2 wafers for As+ implants at 40, 60, and 120 KeV and total doses from 10^{14} to 10^{16}. Photoresist-related effects were studied with the use of dark-field resist patterns intended

to emulate resist layout conditions encountered on CMOS product wafers.

Significant differences in positive and negative charging were observed for different layouts, especially at high implant energies.

As in previous work, a shift toward higher positive charging was observed in the presence of photoresist. Highest positive charging was observed in the case of resist patterns which nearly covered the CHARM-2 charge collection electrodes (the equivalent of transistor gates). Positive charging was significantly lower for patterns where the resist did not cover, or only slightly covered, the charge collection electrodes.

Highest negative potentials were measured on patterns where the resist on the field oxide did not touch the charge collection electrodes. Significantly lower negative potentials were observed on patterns where the resist on the field oxide touched or almost completely covered the charge collection electrodes.

Resist outgassing during the early portion of a S/D implant (10^{14} dose) lead to an increase in negative charging.

Comparison of Implant Charging Results Obtained with QUANTOX and CHARM-2

(S. Daryanani, et. al., Microchip Technology, Tempe, AZ)

A comparison of charging results obtained with Quantox® and CHARM®-2 was presented for the case of Arsenic implants at 80 KeV and 20 KeV, performed at doses of 5e14 /cm2 and 5e15 /cm2 at beam currents of 9 mA and 18 mA on the Applied Materials 9500 xR implanter.

In general, it was determined that Quantox results varied, depending on beam current, dose, ion energy, oxide thickness on the test wafer, and the results did not follow conventional charging models.

For 20 KeV, 4.5e15 implants conducted at the same beam current and beam area, different surface potentials were obtained with Quantox for 800 A oxides and 900 A oxides. While the negative potentials (obtained with PFS ON) scaled approximately in proportion to the oxide thickness, the positive potentials (obtained with PFS OFF) actually decreased with increasing oxide thickness. A very anomalous result.

For 20 KeV, 5e14 implants, conducted at the same beam current and beam area as in the 4.5e15 implants, both positive and negative surface potentials recorded by Quantox were lower, but not in proportion to the implant dose. CHARM-2 results did not depend on the implant dose.

At 80 KeV, only negative potentials were recorded with Quantox, for both PFS ON and PFS OFF, and the results depended on the implant dose. CHARM-2 recorded high negative potentials and low positive potentials with the PFS ON, and high positive potentials and low negative potentials with the PFS OFF, in accordance with conventional charging models, and the results did not depend on the implant dose.

The authors conclude that "although Quantox does provide the potential for quick, in line charge measurements and flag potential deviations in the charge control, an understanding of the limitations placed by the implant beam and energy conditions must be made. A calibration to a known tool such as the CHARM-2 system is essential to get a complete picture of both the positive and negative charge densities that the wafer experiences".

P^{2}ID'98 paper summaries:

Is Surface Potential Measurement (SPM) a Useful Charging Damage Measurement Method?*

(K. P Cheung, et. al., Bell Laboratories, Murray Hill, NJ)

*SPM is implemented in the PDM and Quantox tools (ed.)

In this paper, K. P. Cheung and his eleven co-authors face the facts: "Based upon our experience, this lack of correlation between SPM and plasma charging damage is more common than the apparent correlation that has been reported in the literature."

After presenting several examples to support their case, they conclude that: "the SPM method produces a voltage map that does not always correlate with damage. Since a highly non-uniform or high value SPM map does not imply damage, nor does a uniform and low value map imply no damage, it cannot be used as a damage monitor directly. Until one understands how and where the residual charges are created, the relation between SPM and plasma damage cannot be established." "Unfortunately, such understanding is, at present, missing."

Rapid Detection of Charging Damage with Non-Contact Electrical Analysis

(G. S. Horner, et. al., Keithley Instruments, Santa Clara, CA)

Keithley Instruments also admits that "Despite the well-publicized successes of the Vs mapping method, the user should be aware that each plasma tool and process must be studied to determine whether the surface charge detected by Vs mapping is indeed correlated to actual plasma damage. In addition, low, uniform surface voltages are not sufficient to claim the absence of plasma damage."

"In certain cases, Vs maps may not only fail to detect charging problems, but they may in fact counter-indicate the proper solution to a charging problem."

Note: Although it is valuable to see the experimental evidence, these results are predictable from the physics of the phenomena associated with plasma tools and ion implanters, and were anticipated in WCM's Tech Brief

entitled "SPV/CPD as a tool for monitoring charging damage" (Sept. 9, 1996) which can be obtained from WCM. If you want to understand why the SPM tools sometimes give reasonable results and why often they do not, use CHARM-2 wafers. The responses obtained by the SPM tools can be explained by CHARM-2 data. Or you may avoid the confusion altogether by using CHARM-2.

Charging Damage in Thin Oxides – Better or Worse?

(K. P Cheung, et. al., Bell Laboratories, Murray Hill, NJ)

Here, the authors analyze the influence of measurement conditions and definitions of damage on the often conflicting claims about charging damage to scaled gate oxides in future technologies.

Detailed examination of data obtained on 52A, 34A, and 25A oxides shows that oxide charge-to-breakdown (Q_{bd}) decreases with increasing stress current, and that the decrease is greater for thinner oxides.

It is also known (and very easy to demonstrate with CHARM-2 wafers – ed.) that "older plasma systems belong to the low current, high charging voltage class while modern plasma equipment tends to belong to the high current, low charging voltage class".

Combining these facts, the authors conclude that "the high current and low voltage characteristic of modern plasmas is the main reason for making thinner oxide more prone to charging damage". … It is "the concomitant change to high density plasma processing with advanced technology where thinner gate oxides are used that make plasma charging damage continue to be a major problem".

Note: CHARM-2 is the only tool which conveniently measures both positive and negative charging currents reaching the wafer surface – the underlying cause of gate oxide damage. Isn't it time to prepare for the future, and start using CHARM-2 to monitor your process equipment today?

Transistor Degradation Due To Radiation In A High Density Plasma

(G. Bersuker, et. al., SEMATECH, Austin, TX)

In experiments conducted "in a commercially available HDP oxide etching tool under standard contact etch conditions", the authors observed threshold voltage shifts and transconductance degradation, particularly to NMOS transistors.

It was also observed that "radiation effects exhibit strong dependence on plasma chemistry: exposure to O_2 plasma for 20-100 sec shows no shift in transistor parameters, contrary to the case of C_2F_6 plasma exposure for 30 and 50 sec", and that "the radiation induced shift in G_m did not completely disappear following 30 minute, 400 ^oC anneal".

The authors conclude "that UV radiation during wafer processing can result in degradation of transistor performance and reliability".

Note: CHARM-2 wafers have the ability to separate UV from charging effects, and provide independent measurements of UV intensity and electrostatic charging current densities.

FUTURE TOPICS:

In future issues, we will present case studies of CHARM-2 applications and discuss CHARM-2 application procedures. We will also discuss why device structure can increase or decrease device susceptibility to damage.

If you have topics you'd like to learn about, or would like to contribute material to this bulletin, please contact us.

HOW TO CONTACT WCM:

If you are not on our mailing list, and would like to receive this bulletin or information about our products, services, and publications, please contact:

Wafer Charging Monitors, Inc.
127 Marine Road Woodside, CA 94062
phone: 650-851-9313 fax: 650-851-2252
web site: http://www.charm-2.com
email: sales@charm-2.com

