Wafer Charging Bulletin Vol. 2, No. 1

In this issue …

From the Editor ...

We now distribute this bulletin only by e-mail. Please alert your colleagues to send their e-mail addresses and company name to bulletin@charm-2.com to receive a free copy of this publication.

We are also thinking about establishing a web-based **CHARM-2 users' group** to provide a forum for discussion of CHARM-2 applications and results. Please let us know at users@charm-2.com if this is a good idea, and if you would participate in a CHARM-2 users' group.

New and exciting ...

- In response to customer requests for **a simple method to compare CHARM-2 results to product yield** wafer maps, Wafer Charging Monitors, Inc. introduces **DamageMap™,** which summarizes in a single wafer map the results previously displayed in several maps and J-V graphs. Unlike the surface potential measurement techniques, DamageMap™ produces a wafer map of charging currents, the **real cause** of charging damage. The DamageMap™ maps may be compared directly to product yield wafer maps, to determine if a particular processing tool is responsible for damage to product gate oxide. The underlying principles of this exciting new tool are explained in this issue.

- **CHARM-2 works really well in oxide deposition!** Several unique CHARM-2 features, including the ability to work at temperatures above 400°C, the ability to separate UV effects from charging effects, and the ability to identify charging occurring at elevated temperature vs. at low temperature, provide unmatched ability to analyze and understand charging damage in plasma oxide deposition tools. CHARM-2 succeeded where the competition failed. The details were presented in a 1999 P^2ID paper, which is summarized in this issue.

- **CHARM-2 results correlate to SPIDER damage.** Detailed comparison of CHARM-2 and SPIDER-MEM data shows that device physics must be taken into account when analyzing charging damage results. This comparison also showed that the model used to explain charging damage in high-current ion implanters is not valid for the present generation of tools equipped with plasma-flood charge control systems. A new charging model, and the parameters that are important for charging damage in plasma-flood-equipped high current ion implanters, were presented in a P^2ID paper, and will be discussed in the next issue of this bulletin.

Introducing DamageMap™ …

CHARM-2 J-V plots, which show the net current density collected on the surface of the wafer as a function of wafer surface-substrate potential, are ideal for equipment manufacturers who need to know the damage characteristics of their tools for any gate oxide thickness their customers may use. The intersection of antenna-ratio-multiplied CHARM-2 J-V plots and the Fowler-Nordheim (F-N) oxide conduction plots provide this information, as shown in Figure 1.

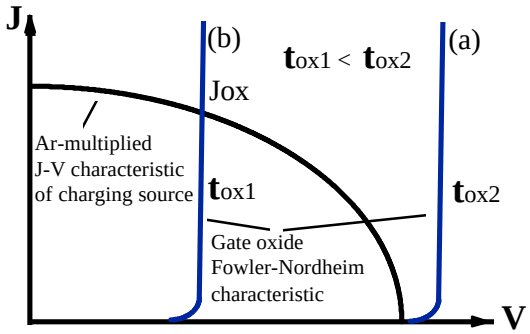

Figure 1. Oxide damage prediction: **(a)** F-N plot does not intersect A.R.-multiplied JV plot: damage is not possible; **(b)** F-N plot intersects A.R.-multiplied JV plot: damage is likely. (Note: A.R. = Antenna Ratio.)

If the customer's gate oxide F-N plot does not intersect the CHARM-2 J-V plot, the tool will not cause charging damage to the customer's gate oxide. (This topic was discussed in detail in Wafer Charging Bulletin, Vol. 1, No. 1, which can be downloaded from our web site.

However, for purposes of comparison with product yield wafer maps, J-V plots are cumbersome since 355 J-V plots are needed to completely describe the charging characteristics on a 200 mm wafer (one J-V plot for each die location). What is needed for comparisons with product yield wafer maps is a **single wafer map which**

shows the values of the damage-producing oxide current density, Jox, obtained at the intersection of the product-specific gate oxide F-N plot with the process tool J-V plots at each die location. This is precisely what **DamageMap™** provides.

Before DamageMap™ became available, IC makers attempted to use surface potential wafer maps, which sometimes correlated to product damage wafer maps, but often did not[1]. This is to be expected, since the amount of charge needed to reach significant surface potentials is several orders of magnitude lower than the breakdown charge of the oxide[2]. Consequently, high surface potentials do not always lead to damage. Moreover, the region of maximum surface potential is often not the region of maximum oxide current density responsible for device damage[3], as illustrated below with an example from oxide deposition.

Figure 2 shows the map of surface-substrate potentials obtained with CHARM-2 ChargeMap®.

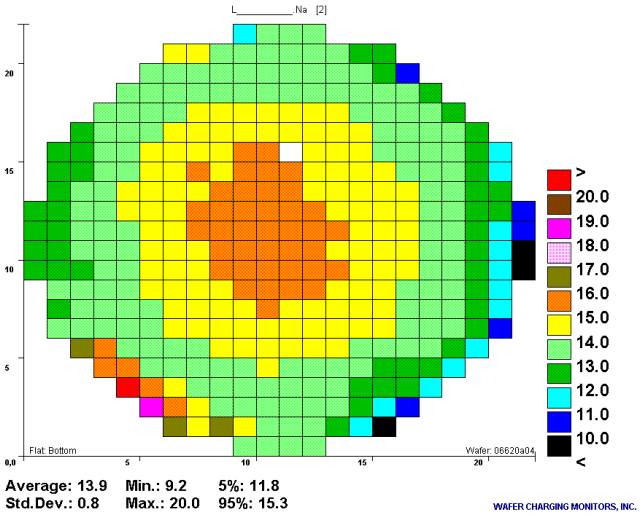

Figure 2. ChargeMap® of surface-substrate potentials in oxide deposition.

Although the peak surface-substrate potentials occur in the center of the wafer, maximum positive current density reaching the surface of the wafer occurs in the upper-left of the wafer, as shown in Figure 3.

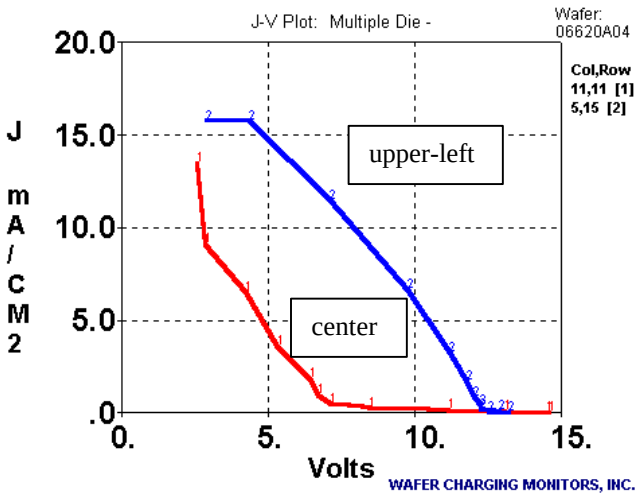

Figure 3. Positive current density in the center and upper-left of the wafer.

Consequently, maximum charging damage occurs in the upper-left of the wafer, as indicated by the DamageMap™ wafer map of the oxide positive current density shown in Figure 4, **not** in the center of the wafer, as might be suggested by the potential wafer map in Figure 2. (In this analysis, a gate oxide breakdown voltage of 10 V was used. Similar wafer maps could be obtained for other oxide breakdown voltages.)

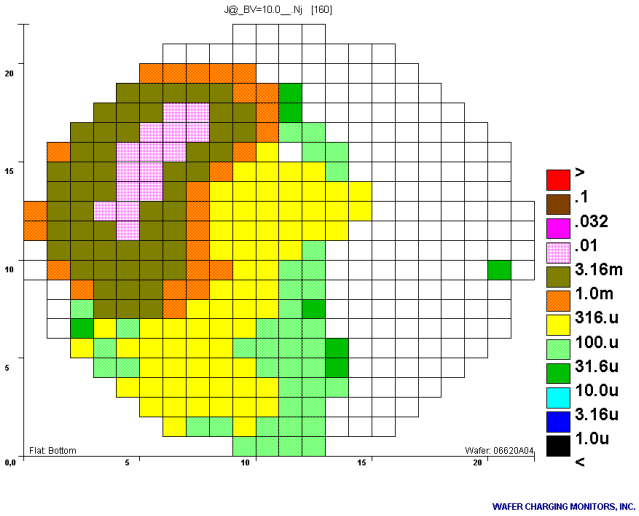

Figure 4. DamageMap™ of net positive current density in A/cm^2 (at BV_{ox} = 10 V) reaching the surface of the wafer.

The DamageMap™ wafer map from a given process tool may thus be compared directly to product yield maps. If the DamageMap™ result correlates to the yield loss wafer map, and the current densities indicated in the DamageMap™ are high, the tool is a likely suspect.

Since gate oxide Fowler-Nordheim (F-N) plots are sometimes not available in wafer fabs, but gate oxide

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[1] K. P. Cheung, et al, "Is Surface Potential Measurement (SPM) a Useful Charging Damage Measurement Method?", 1998 3rd International Symposium on Plasma Process-Induced Damage, p.18, June 4-5, 1998, Honolulu, Hawaii.

[2] To develop 10 V on a 100 nm oxide, a surface charge of 3.5e-7 coul/cm^2 is required. This is about 7 orders of magnitude lower than the charge required to break down a typical gate oxide, and about 4-5 orders of magnitude lower than the charge required for the onset of change in surface state density.

[3] When it comes to sources of electric charge, voltage and current are two independent variables. The magnitude of one says nothing about the magnitude of the other!

breakdown voltage data are, DamageMap™ uses the oxide breakdown voltage as the input variable. This is acceptable since charging damage in process tools occurs in seconds, and thus at a high current-density which occurs at nearly the breakdown voltage of the oxide. Since product loss is likely due to failure of the weakest device in the IC, the breakdown voltage used in DamageMap™ should correspond to the lowest breakdown voltage observed in a large sample of gate oxide tests.

DamageMap™ is now available from Wafer Charging Monitors, Inc. Please contact sales@charm-2.com for more information.

Charging in oxide deposition:

The following describes a case-study of charging damage in a plasma oxide deposition tool. The findings summarized here were first presented at the 1999 4th International Symposium on Plasma Process-Induced Damage (P2ID'99) by Ming-Yi Lee, et al, from LSI Logic Corporation. The paper was entitled **"Comparison of CHARM-2 and Surface Potential Measurement to Monitor Plasma Induced Gate Oxide Damage".**

This investigation was prompted by unacceptable burn-in results in early stages of process development. The failures, associated with gate oxide damage, came from the center of the wafer. A surface potential measurement (SPM) wafer map, shown in Figure 5, implicated a resist asher, but product split lots did not confirm this.

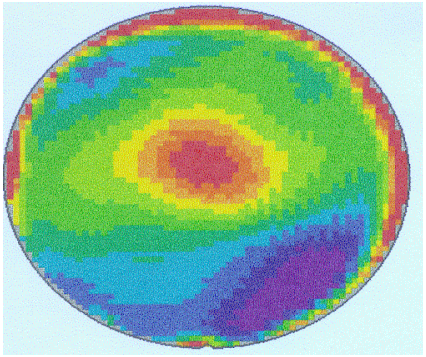

Figure 5. SPM positive potentials in the resist asher.

CHARM-2 wafers were also employed to investigate the cause of gate oxide damage. Although high potentials in the center of the wafer were also observed with CHARM-2 in the resist asher, the current density was low. This suggested that the asher may not be the cause of the problem.

The oxide deposition tool was not suspected because its SPM map indicated a gradient across the wafer, as shown in Figure 6, which did not correlate with the locations of the devices which failed burn-in. However, CHARM-2 recorded moderate positive potentials in the oxide deposition tool in the center of the wafer, as shown in Figure 7.

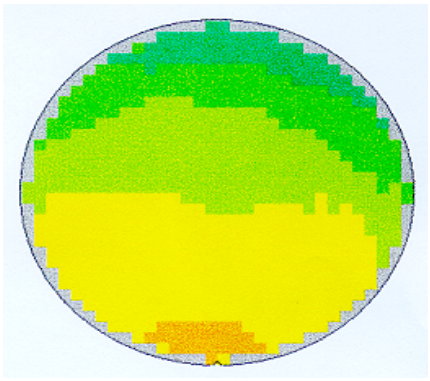

Figure 6. SPM negative potentials in the oxide deposition tool.

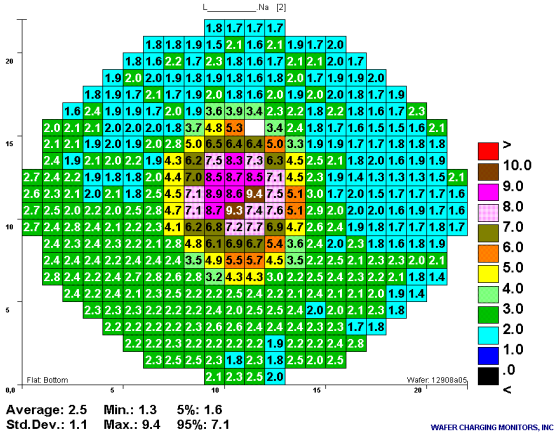

Figure 7. CHARM-2 map of positive potentials in the plasma oxide deposition tool.

Moreover, the CHARM-2 positive J-V plots indicated very high current densities in the center of the wafer, as shown in Figure 8. This caused the oxide deposition tool to become the focus of the investigation.

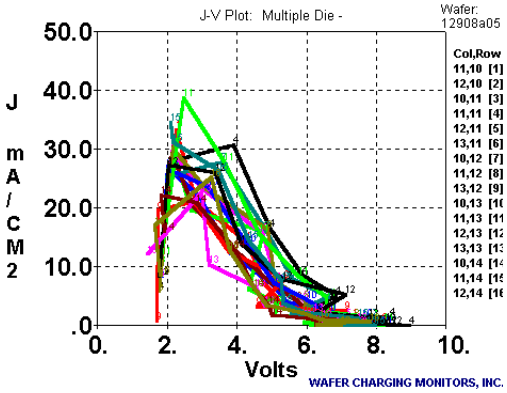

Figure 8. CHARM-2 positive J-V plots n the plasma oxide deposition tool.

Additionally, it was observed that CHARM-2 positive J-V plots obtained with the unipolar charge-flux sensors, shown in Figure 9, were shifted to lower voltages, as shown in Figure 10. This could only happen if the diode leakage current was very high, which could only occur at a high temperature. Consequently, this observation

confirmed that the high positive current densities shown in Figure 8 were associated with the oxide deposition process.

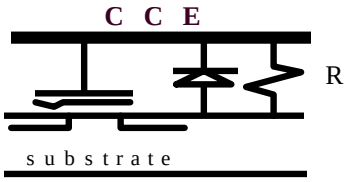

Figure 9. CHARM-2 unipolar positive charge-flux sensor: CCE = charge collection electrode; R = current sensing resistor. (The charge-flux sensors used to obtain the J-V plots in Figure 8 do not use a diode.)

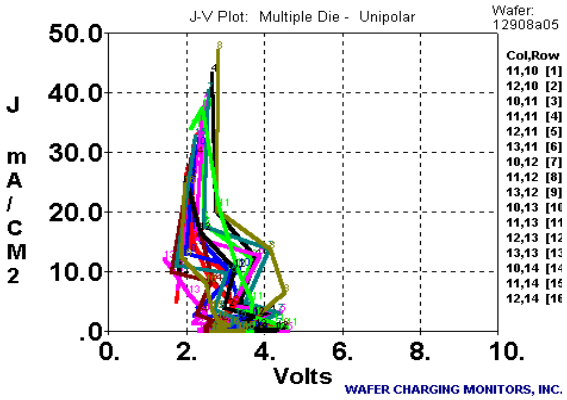

Figure 10. CHARM-2 positive J-V plots obtained in the oxide deposition tool with the unipolar charge-flux sensors.

Subsequent experiments with the oxide deposition system, and the use of CHARM-2 wafers as monitors, lead to the development of a benign process which eliminated the burn-in fails problem.

A gradient in negative potentials, similar to those obtained with SPM in Figure 6, was also recorded with CHARM-2 wafers, as shown in Figure 11.

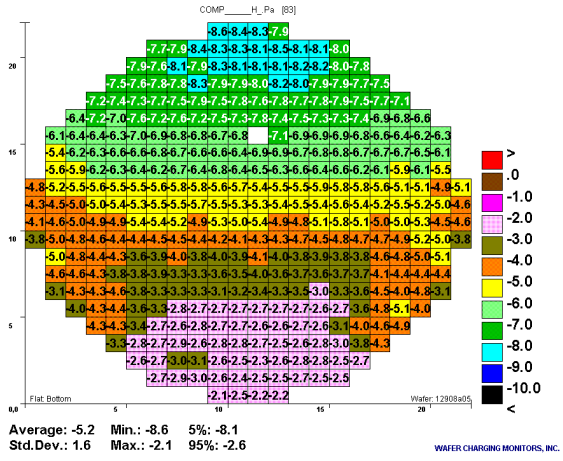

Figure 11. CHARM-2 map of negative potentials in the plasma oxide deposition tool.

However, the negative J-V plots showed negligible current densities (compared to positive J-V plots), and virtually identical J-V plots were obtained with both types of charge-flux sensors. This demonstrated that negative charging could not be the cause of the problem, and that negative charging occurred at low temperature, after oxide deposition. Subsequent experiments showed that the negative charging was associated with the wafer moving out of the deposition chamber while the plasma was still on. When the plasma was turned off before moving the wafer, the SPM also recorded a bulls-eye pattern.

These results confirmed that the SPM recorded only the last charging event and could not distinguish between charging at high temperature and low temperature. On the other hand, **CHARM-2 wafers recorded all charging events that occurred during this multi-step process, and distinguished between charging at high temperature and low temperature, thus providing unmatched diagnostic capability.**

MORE ON P2ID'99

To learn about other recent findings published at the 1999 4th International Symposium on Plasma Process-Induced Damage (P2ID'99), please visit our web site at http://www.charm-2.com and click on "Latest Research!"

FUTURE TOPICS:

In the next issue, we will review additional papers from P2ID'99. In particular, we will discuss how device structure can increase or decrease device susceptibility to damage. We will also review recent work on the relationship between UV and device damage.

If you have topics you'd like to learn about, or would like to contribute material to this bulletin, please contact us.

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