Wafer Charging Bulletin

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In this issue …

From the Editor ...

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New and exciting ...

- **CHARM^{Ò}-2 automated data analysis!**

CHARM-2 data analysis is now completely automated! The latest release of ChargeMap generates the appropriate wafer maps, J-V plots, and a page-long report automatically – a click on the "Analyze" button does it! The new ChargeMap also verifies the integrity of the calibration, program, and measure data files to ensure a fool-proof assessment of the charging characteristics of your process tools. The new ChargeMap is available now, and will soon be released (free) to all previous ChargeMap owners.

- **Additional test capability!**

WCM recently implemented additional, on-site testing of CHARM-2 wafers. This new capability improves WCM's turn-around time for CHARM-2 analyses – second-day response is now typical – and emphasizes WCM's commitment to speedy service.

- **Maximum-response CHARM-2 wafers!**

WCM's investigations of wafer charging phenomena led to the observations that charging monitors do not provide a unique measurement, and that charging monitor response can be tailored over a significant range. In view of these findings, which have been published and are discussed in more detail below, WCM now offers CHARM-2 wafers whose response is tailored to provide "worst-case" measurements. These new designs complement the standard CHARM-2 wafers whose balanced characteristics are still best for all-purpose applications.

The sense and non-sense about charging damage …

In spite of the volumes of published papers on wafer charging damage, and a variety of measurement techniques used to analyze it, charging damage is still a source of confusion to many engineers.

In the following, we review selected publications from P^{2}ID'2000 and IIT'2000, discuss the variables that influence monitor response, and try to sort out what's important and what's less important about charging damage and wafer charging measurements. Finally we discuss how CHARM-2 charging monitors can be used in all types of wafer processing tools.

"Electron shading" – how important is it?

Given the large number of papers published about "electron shading" damage and mechanisms [1], one might conclude that "electron shading" must be the dominant cause of wafer charging damage. How accurate is this impression? How significant is this mechanism?

To answer the latter, J.-P. Carrere [2] used a CHARM-2 wafer to measure the "electron shading" induced potentials and current densities in an oxide etcher. The CHARM-2 wafer was covered with 0.6 um photoresist and exposed by e-beam lithography to produce a variety of hole and line patterns with dimensions ranging from 0.6 um to 0.15 um. The wafer was then exposed to a high-density plasma in an ICP chamber. A bare CHARM-2 wafer exposed to the same process served as a reference.

The positive potentials recorded with the bare wafer were low (~ 2 V) and uniform, indicating good plasma uniformity. The positive potentials recorded with the patterned CHARM-2 wafer are shown in Figure 1. The different values obtained in different die locations correspond to different resist patterns. It is evident that the presence of resist patterns causes high potentials to be developed in the resist openings.

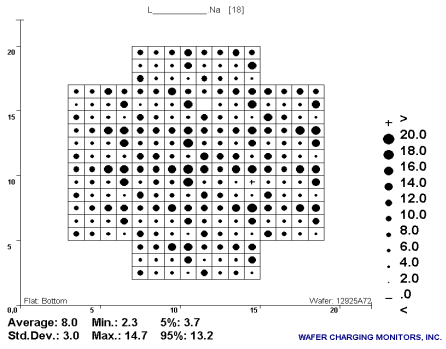

Figure 1. Positive potentials caused by "electron shading" in HDP oxide etcher.

Figure 2 shows positive J-V plots obtained with patterns containing 0.6 um, 0.3 um and 0.15 um holes. The peak potentials increase with decreasing size, and the current densities are very high. Clearly, the "electron shading" effect is real (although there exist other ways to elevate potentials and current densities, as we shall see later).

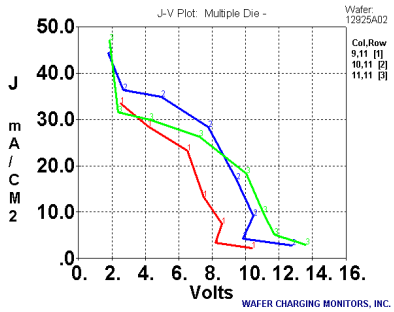

Figure 2. Positive current density caused by "electron shading" in HDP oxide etcher. Curve "1" corresponds to 0.6 um holes; curve "2" corresponds to 0.3 um holes; curve "3" corresponds to 0.15 um holes.

But is "electron shading" the *dominant* charging damage mechanism during wafer manufacturing? Simple logic, and our own observations, suggest that it is not. "Electron shading" is a fundamental mechanism associated with plasmas, and its magnitude depends on the aspect ratio of the resist features. Consequently, in uniform plasmas it should produce uniform damage in all die on the wafer. Manufacturing yield data indicates otherwise. Typically, charging damage is not uniformly distributed, but is confined to some region of the wafer.

The push "over the cliff": plasma non-uniformity!

This is consistent with the observations WCM accumulated during our six years of working with customers suffering from charging damage problems. Typically, customers work with bare CHARM-2 wafers, which are insensitive to "electron shading", but which provide a very detailed assessment of plasma non-uniformity. Whenever charging damage is present, so is plasma non-uniformity. We have observed this countless number of times. This does not imply that "electron shading" is not important, but it does indicate that in product manufacturing situations[1] it is plasma non-uniformity that ultimately "pushes things over the edge of the cliff".

As explained in WCM technical literature, CHARM-2 excels in quantifying plasma or ion-beam induced charging non-uniformities. It provides separate maps of wafer surface-to-substrate potentials, positive and negative J-V plots, and distribution of UV emissions in a process chamber – significantly more than any other charging monitor. Still, quantifying the magnitude of plasma charging non-uniformities is more complex than it was thought previously. This is due to the interaction of the wafer with the process environment: the magnitude of surface-to-substrate potentials experienced by device structures results from the interaction between the ***entire*** wafer and the process environment. Structures of interest are **not** the only ones responsible for the observed results. Their neighbors also exert an influence due to their connections to the substrate, which modulates the substrate potential, thereby modulating the surface-to-substrate potentials.

In a paper presented at IIT'2000 [3], W. Lukaszek showed that connecting different size charge-collection antennas to wafer substrate shifted the position of ion implant J-V plots along the surface-to-substrate potential axis, as shown in Figures 3a and 3b. Larger antennas decreased the positive surface-to-substrate potentials and increased the negative potentials. Conversely, smaller antennas increased the positive surface-to-substrate potentials and decreased the negative potentials.

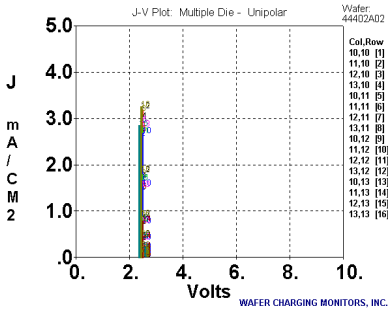

Figure 3a. Positive J-V plots recorded in the center of a bare CHARM®-2 wafer with large charge collection area connected to the substrate. The vertical line at ~ 2.3 V indicates that the charge-flux sensors did not respond, i. e., positive potentials were less than ~ 2.3 V.

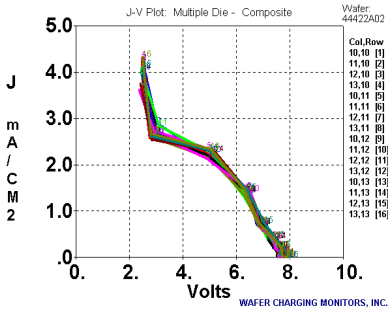

Figure 3b. Positive J-V plots recorded in the center of a bare CHARM®-2 wafer with small charge collection area connected to the substrate. Peak potentials of ~ 8 V were recorded. (The vertical asymptote at ~ 2.4 V is an artifact of the data conversion procedure, and should be ignored.)

Similar observations were made in plasma equipment [4], although different behavior was observed in different tools. Figures 4a and 4b show the positive potentials obtained with CHARM wafers with and without scribe lane PCM monitors. An opposite response was observed in a different plasma tool, as shown in Figures 5a and 5b, illustrating the complexity of behavior encountered in plasma equipment.

In experiments conducted in oxide etchers using bare CHARM wafers with different size charge-collection antennas connected to substrate (as in Figures 3a and 3b), elevated positive potentials and positive current densities were observed on wafers with small antennas connected to substrate[2]. Since the placement of resist masks over a wafer can also reduce the charge collection area connected to wafer substrate [5], some of the damage attributed to "electron shading" may actually have been due to the reduction of open ("unshaded") areas connected to substrate.

[1] Although "electron shading" damage is observed on test structures, the likelihood of observing "electron shading" damage on products is reduced by design rules which limit the size of charge collecting antennas.

[2] To be published.

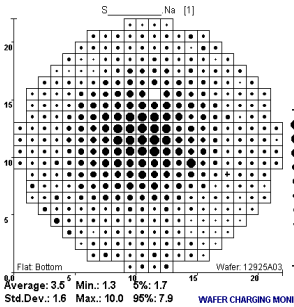

Figure 4a. Positive potentials recorded in a plasma tool #1 with a bare CHARM®-2 wafer containing scribe-lane process control structures.

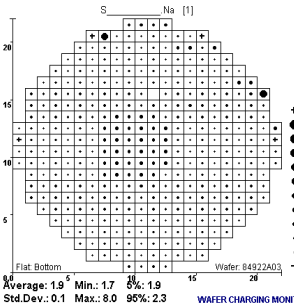

Figure 4b. Positive potentials recorded in a plasma tool #1 with a bare CHARM®-2 wafer without scribe-lane process control structures.

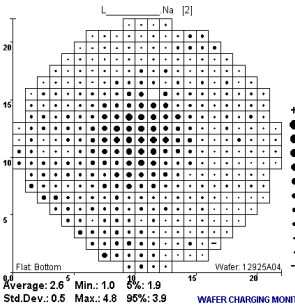

Figure 5a. Positive potentials recorded in plasma tool #2 with a bare CHARM®-2 wafer containing scribe-lane process control structures.

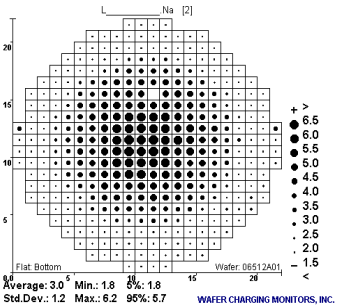

Figure 5b. Positive potentials recorded in a plasma tool #2 with a bare CHARM®-2 wafer without scribe-lane process control structures.

These observations indicate that charging stress experienced by devices in a chip can be modulated in many ways, even by seemingly inconsequential structures such as scribe lane devices. For these reasons, different products can experience different charging stress even when processed in identical tools, under identical process conditions[3]. Clearly, surface-to-substrate potentials are not absolute, but depend on the presence, or absence, of resist features, chip device content, and connections to substrate.

Let's not forget about UV !

Although the role of UV in charging damage has not been studied extensively (probably due to wide-spread use of monitors which can not distinguish between UV and charging effects), recent P2ID papers (and our own data) clearly indicate that UV alone can produce damage, or that it can enhance damage by working synergistically with wafer charging [6,7]. As K. P. Cheung pointed out, a particularly important case of UV-assisted charging damage occurs during dielectric deposition [8]. The UV causes the deposited oxide to conduct current, which is collected by conductors (antennas) under the oxide. Since the high deposition temperature greatly lowers the charge-to-breakdown of the gate oxide, this current is sufficient to cause damage even to small antenna-ratio devices.

Getting the most from charging monitors

From these discussions, we see that ***all*** charging monitors provide a ***relative*** measurement. Even damage monitors[4] (antenna devices), frequently perceived as the absolute truth, provide a *relative* measurement which depends on the devices they contain and their connections to the substrate. In fact, damage monitors can mislead because they ***require*** high surface-to-substrate potentials to inject charges into the gate oxide in order to register damage[5]. If the surface-to-substrate potentials are insufficient to do this, no damage is recorded[6]. But the CHARM results presented here show that surface-to-substrate potentials can be modulated over a large range by changing the amount of charge collecting area connected to the substrate. Consequently, it is possible to design different damage test chips which use the same antenna ratio devices and find that, under identical process conditions, some of them register damage while others do not!

Recognizing that charging monitors provide a ***relative*** measurement of the variables responsible for charging damage leads to the realization that there is a correct and an incorrect way to use charging monitor data. The incorrect way is to use charging monitor results to "prove" that a given process tool can or cannot cause damage. In view of the results presented here, "prove" should be softened to "suggests". Of course, after correlation to product damage is established, charging monitor results **can** be used with confidence to qualify tools for production.

Charging monitor results can also be used with confidence to compare different tools of the same make and model. Comparing tools of similar design can also be done with reasonable confidence. However, plasma tools of significantly different design or function should be compared with caution, since a particular monitor may not respond in the same way in different tools, as shown in Figures 4a-5b. In such cases, pairs of monitors[7] optimized to provide maximum/minimum response, such as those now provided by WCM, should be used.

In general, the best philosophy is to use monitor results as ongoing means to improve tools and processes whenever charging is detected. For this application, relative measurements are adequate provided that (a) the monitor used responds to all variables which can cause product damage; (b) the monitor provides high measurement resolution (and good spatial resolution) in order to detect relevant changes in tool charging characteristics; (c) the monitor is able distinguish and separately measure the

[3] Of course, it may also be possible to use this behavior to *reduce* charging stress …

[4] Due to their ill-defined response, and lack of resemblance to ICs, contactless techniques are not considered relevant in this discussion.

[5] Additional measurement difficulties arise for very thin gate oxides (< 30 A).

[6] Except in the case of UV-assisted damage during oxide deposition, as discussed previously.

[7] Since a monitor optimized to provide a maximum response in a particular tool may provide a minimum response in another tool, and vice versa, both monitor types are needed initially to establish the charging characteristics of a given tool. From then on, only the maximally-responding monitor can be used.

different variables responsible for product damage (potentials, current densities, and UV) because different causes may require different remedies; and (d) the monitor provides reproducible results.

As explained in WCM technical literature, the CHARM-2 charging monitors satisfy all of these requirements. What is often not clear to our new customers are the CHARM-2 application procedures appropriate for the different process tools used in wafer manufacturing. During the past six years, WCM has helped customers measure the charging characteristics of all types of process tools used in wafer manufacturing. In the course of doing this, we have developed some simple guidelines, as described below.

CHARM-2 application procedures

Since charging damage is typically associated with large-area charging non-uniformities, virtually all charging damage reduction work can be carried out with bare CHARM-2 wafers. The proper application procedures for the different processes are as follows:

• **Resist ashing:** Since resist ashing does not remove any material from the surface of a wafer, CHARM-2 wafers may be exposed to the ashing plasma for the entire duration of the ashing cycle, just like product wafers. In multi-wafer ashers (such as barrel ashers) position of the wafer in the load is often important!

• **Ion implantation:** Since ion implantation does not remove material from the surface of a wafer, CHARM-2 wafers may be exposed to the entire ion implant, just like product wafers. To observe resist-modulated changes in tool performance, the other wafers on the wheel may be resist-covered product wafers. Otherwise, tool performance and tool stability are best monitored when the "dummy" wafers are not coated with resist.

• **Plasma etching (including ion milling):** Since etching processes remove material from wafers, they can be lethal to CHARM-2 wafers. Metal etching is most dangerous since it can remove the probe pads, making it impossible to read-out the acquired information. Fortunately, the CHARM-2 EEPROM-based sensors respond in less than a millisecond. Therefore, a short exposure to etching plasma is sufficient to capture the charging and UV emissions characteristics of the plasma. To ensure that both the transient and steady-state of the plasma are adequately characterized, the exposure time should be sufficient for the plasma to reach a steady-state. In most cases, a 5 to 10 second exposure is adequate.

• **Oxide deposition:** Since it is essential to remove all deposited oxide from CHARM-2 wafers in order to read-out the acquired information, the deposition cycle should be as short as possible. To ensure that both the transient and steady-state of the plasma are adequately characterized, the deposition time should allow the plasma to reach a steady-state. In most cases, a 5 to 10 second deposition is adequate. The deposited oxide can be removed with plasma or a wet etchant. If it is removed with a plasma, the system used should first be characterized with a CHARM-2 wafer to ensure that the oxide removal process does not cause charging. If the deposited material is removed with a wet etchant, an ammonium-fluoride-buffered HF (BHF) solution should be used, since it is significantly less aggressive toward the Aluminum metalization on CHARM-2 wafers than water-HF solutions. To further reduce the etching of the metalization on CHARM-2 wafers, the overetch time in the BHF solution should be minimized. This can be accomplished by calibrating the BHF etch time using a bare silicon wafer which received the same deposition as the CHARM-2 wafer.

• **Metal deposition:** Since metal deposition will short all probe pads on the CHARM-2 wafer, it is essential to remove the deposited metal from the CHARM-2 wafer in order to read-out the acquired information. To facilitate this, the deposition cycle should be as short as possible. To ensure that both the transient and steady-state of the plasma are adequately characterized, the deposition time should allow the plasma to reach a steady-state. In most cases, a 5 to 10 second deposition is adequate. The deposited metal can be removed with plasma or a wet etchant. If it is removed with a plasma, the system used should first be characterized with a CHARM-2 wafer to ensure that the metal removal process does not cause charging. If the deposited material is removed with a wet etchant, the overetch time in the metal-etch solution should be minimized. This can be accomplished by calibrating the etch time using an oxidized silicon wafer which received the same deposition as the CHARM-2 wafer.

• **Other processes:** Contact WCM for recommendations.

References:

[1] K. Hashimoto, Jpn. J. Appl. Phys., 33 (1994) 6013.
[2] J.-P. Carrere, et al, P2ID'00, pp. 22-25.
[3] W. Lukaszek, IIT2000
[4] W. Lukaszek, P2ID'00, pp. 26-28.
[5] W. Lukaszek, et al, P2ID'96, pp. 30-33.
[6] C. Cismaru, J. Shohet, and J. McVittie, P2ID'99, pp. 192-195.
[7] S.-S. Lin, S-S., et al, P2ID'99, pp. 41-44.
[8] K. P. Cheung, P2ID'00, pp. 161-163.

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