Wafer Charging Bulletin

Vol. 4, No. 1

In this issue …

- **From the Editor …**
- **New and exciting …**
- **Diagnosing plasma charging problems …**

From the Editor ...

• **We now distribute this bulletin only by e-mail**. Please alert your colleagues to send their email addresses and company name to bulletin@charm-2.com to receive a free copy of this publication.

• **Typical charging patterns and what they mean:** in this issue we discuss the various kinds of charging problems encountered in plasma-based processing equipment, and how to identify them using CHARM-2 wafer maps and J-V plots.

New and exciting ...

- **Additional test capability!**

WCM is implementing additional on-site testing capability for CHARM-2 wafers, emphasizing WCM's commitment to next-day turn-around for CHARM-2 analysis services.

Diagnosing Plasma Charging Problems with CHARM-2 …

Most charging damage problems in IC manufacturing occur in plasma tools used to deposit and etch dielectric and metal layers[1]. Our work using CHARM-2 wafers covered with resist patterns [1] makes it clear that plasma non-uniformity greatly enhances "electron shading" damage associated with high aspect ratio topographies during back-end processing. Consequently, eliminating plasma non-uniformity through hardware or recipe changes eliminates charging damage. The following is a brief look at the kinds of problems typically encountered in back-end process tools, and how they can be identified using CHARM-2 wafers. A brief description of CHARM-2 wafer application procedures is also included at the end of this tutorial.

Introduction

CHARM-2 wafers contain UV, potential, and charge-flux sensors. The UV sensors are integrating sensors, while the potential and charge-flux sensors are peak-detectors which "remember" the peak voltages and currents detected at any time during the ***entire*** process sequence. This set of sensors thus provides a ***complete*** overview of ***all*** charging phenomena that occurred in the process tool. Sometimes, the set of responses is simple, pointing to a single offending step. Often, it is more complex, indicating multiple problems – whose identification may require additional experiments using processes which are subsets of the full process recipe. The following examples illustrate the range of complexity encountered in contemporary process tools. We hope they will help CHARM-2 users to understand – and to make better use of – their CHARM-2 results.

Simple non-uniform plasmas

The simplest case of a non-uniform plasma in a process tool is the instance where only one of the several process sub-steps exhibits a plasma non-uniformity problem. This case is easily identified by the complementary relationships – dictated by plasma physics – that exist between the UV map, the positive and negative potential maps, and J-V plots, as illustrated in Figures 1-5.

In a high density plasma (HDP), the region of lower UV emissions is associated with higher plasma density[2], which gives rise to greater positive charging. Consequently, the UV map and the positive potentials map are complementary – where one exhibits high values, the other one exhibits low values, as shown in Figures 1 and 2.

In order to cause device damage, current must flow through gate oxide. Since the chuck is electrically floating, damage-causing current must flow from the plasma into the substrate in one region of the wafer, and out of the substrate back into the plasma in some other region of the wafer. For this to occur, the plasma must support positive surface-substrate potentials in one portion of the wafer, and negative surface-substrate potentials in another portion of the wafer. Consequently, the positive and negative potentials maps are also complementary, as shown in Figures 2 and 3.

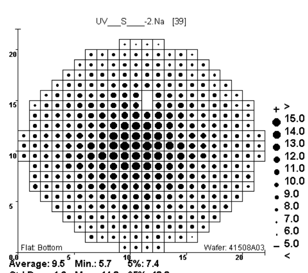


Fig. 1. HDP: UV response.

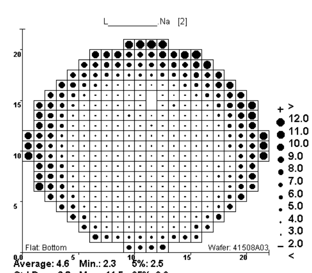


Fig. 2. HDP: Positive potentials.

[1] Although wafer charging can also occur in the "front-end" of the IC process, the damage – provided it does not lead to gate-oxide rupture – is typically annealed out during the high-temperature S/D ion implant anneal.

[2] Conversely, in low density plasmas the region of higher UV emissions is associated with higher plasma density.

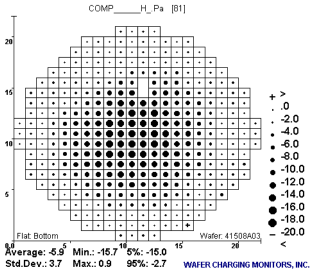


Fig. 3. HDP: Negative potentials.

Note: The complementary nature of the UV and potential patterns is the reason why spatial correlations are observed between charging damage and SPM maps in cases of simple, non-uniform plasmas. Such spatial correlations will be observed whether the SPM readings are from UV or from charging phenomena.

The complementary nature of the current flow paths is illustrated by the J-V plots shown in Figures 4 and 5. In this case, current entered the substrate around the periphery of the wafer and left through the center of the wafer. Note that the voltages recorded on the positive and negative J-V plots at J=0 are precisely the voltages recorded around the periphery of the positive potential map (Fig. 2) and at the center of the negative potential map (Fig. 3), respectively. This is expected, since potentials are measured with very high input impedance sensors, which draw virtually no current.

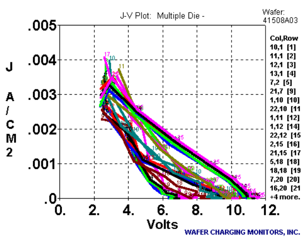


Fig. 4. HDP: Positive J-V from wafer periphery[3].

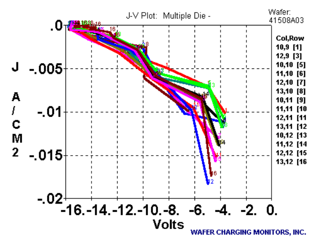


Fig. 5. HDP: Negative J-V from wafer center.

This consistency of patterns recorded in the UV maps, potential maps, and J-V plots indicates a single cause. Eliminating it will eliminate charging damage. However, it should be recognized that the complementary patterns illustrated in this example may take different forms in different tools. For example, gradient patterns are frequently observed where one side of the wafer shows low UV and high positive charging, while the opposite side of the wafer shows high UV and high negative charging.

Unstable plasmas

Unstable plasmas present a great challenge to diagnose properly, since the damage they can cause may be confused with random defects produced by other sources. The reason for this is illustrated in Figures 6-8.

Figure 6 shows the negative potentials obtained with a particular potential sensor. High negative potentials are recorded in some die, but their locations appear to be random, unlike the systematically distributed values in the previous example. However, when the maximum value from four identical sensors is displayed, as shown in Figure 7, it becomes clear that intense charging activity occurred in the center of the wafer. Since the physical separation between different sensors is on the order of a couple of millimeters, this indicates that the individual charging events were highly localized.

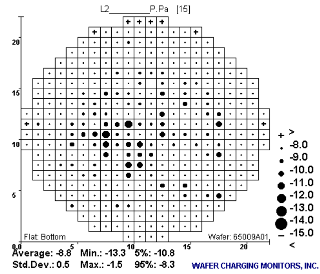


Fig. 6. Unstable plasma: Negative potentials obtained with a single potential sensor.

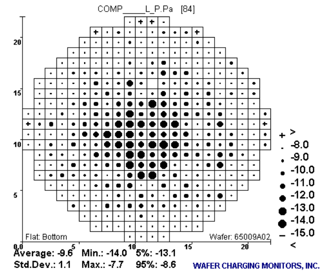


Figure 7. Unstable plasma: Negative potentials obtained with multiple potential sensors.

The irregular ("zig-zag") nature of the negative J-V plots (obtained by combining data from many sensors in each die), shown in Figure 8, indicates that each sensor responded to a very different charging environment. This confirms the highly localized nature of the negative charging events. Moreover, the magnitude of the negative current density is high, indicating that the negative charging events were very capable of causing device damage.

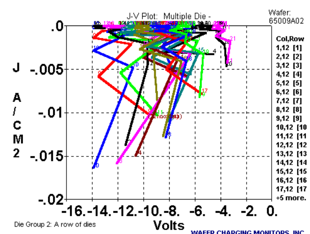


Figure 8. Unstable plasma: Negative J-V plots.

Fortunately, unstable plasmas are rarely encountered in processes used in wafer manufacturing. The first step in dealing with such processes is to eliminate the instability through recipe change. After plasma stability has been achieved, one should proceed to eliminate any remaining plasma non-uniformities.

Complex charging patterns

Often, a complex charging response is recorded in which the complementary relationship between UV, potential wafer maps, and J-V plots is not observed. This does not mean that the tool does not obey plasma physics. It simply means that the recorded response is a complex composite of several events. These events may occur one after the other – for example, when one charging step follows another – or they may occur as result of interactions between steps, such as interactions between process plasmas and the electrostatic chuck during transitions from one process step to another.

An example in which damaging positive charging in plasma deposition was followed by benign negative charging during wafer transport was described by M-Y Lee at P2ID'99 [2]. A complementary relationship between the UV map and the positive potential map was observed, as shown in Figures 9 and 10, indicating that both came from the same process step. Very high positive current densities were also recorded in the center of the wafer, as shown in Figure 11. The peak

3 We use here the EE sign convention: current carried by positive charges enters the positive terminal.

positive potentials recorded in the J-V plots matched the potentials recorded in Figure 10, indicating that the same positive charging source was responsible for both.

However, the negative potential map, shown in Figure 12, showed no relationship to the positive potential map, indicating that negative charging occurred either before or after the positive charging event, and was not due to the same source as positive charging. Nonetheless, the descending progression of peak voltages in the negative J-V plots, shown in Figure 13, matched the negative potentials in Figure 12, indicating that both negative potentials and negative currents could be attributed to the same source.

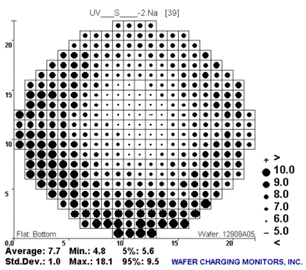


Fig. 9. Oxide deposition:
CHARM-2 UV response.

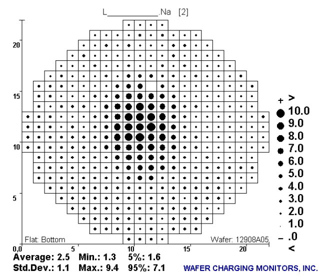


Fig. 10. Oxide deposition:
CHARM-2 UV Positive potentials.

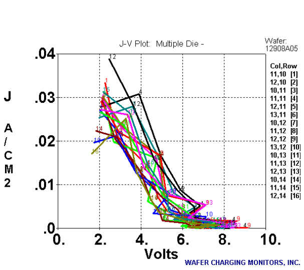


Fig. 11. Oxide deposition:
Positive J-V from wafer center.

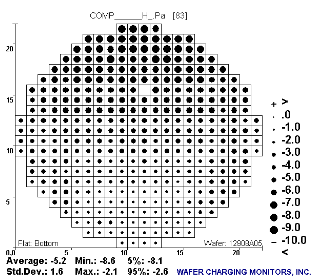
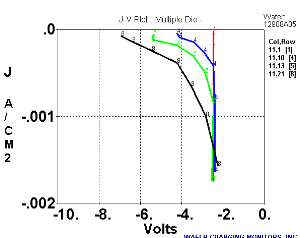


Fig. 12. Oxide deposition:
CHARM-2 Negative potentials.



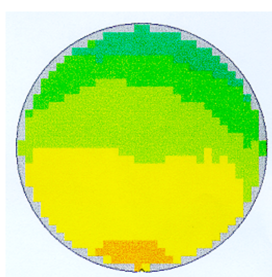


Fig. 13. Oxide deposition:
Negative J-V: top to bottom.

Fig. 14. Oxide deposition:
SPM map.

When the CHARM-2 negative potentials map was compared to a SPM map, shown in Figure 14, it became apparent that positive charging occurred first, followed by negative charging[4]. Subsequent experiments confirmed that the negative charging resulted from movement of the wafer from one process chamber to another. Since the burn-in failures caused by this tool came from the center of the wafer, as would be expected from the high positive current densities, the damaging event was the positive charging event – which the SPM technique failed to detect.

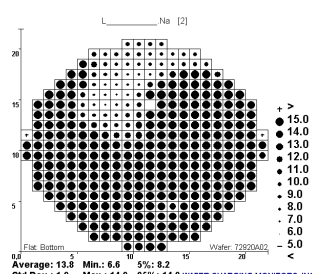
A really complex charging pattern!

An investigation of a very complex charging response obtained from an interaction between process plasma and the electrostatic chuck during a contact etch process in the TEL Unity 85 DRM MERIE oxide etcher was recently presented by M. Kobayashi at the ECS Semiconductor Technology Conference [3] in Shanghai.

Figures 15 and 16 show the peak positive and negative potentials – which clearly bear no relationship to each other, indicating their un-related origins. The positive potential sensors were saturated, indicating that peak positive potentials exceeded 15V. However, the voltages in the positive J-V plots were significantly lower than 15V, indicating that the charging source responsible for the positive potentials in Figure 15 was not the source responsible for the positive J-V plots!

Furthermore, the shapes of the positive J-V plots in Figure 17, obtained from four die in a column through the center of the wafer, indicate that at least three different positive charging events occurred during this process. One event is characterized by curve 1 (red). Another event is characterized by curve 3 (green). In some locations these two events overlapped, giving rise to curve 4 (black). However, in the lower center of the wafer, neither of these events was recorded, as indicated by the blue vertical line at 2V. In fact, positive current density was less than $0.8\mu A/cm^2$ (the "no-response" level), but the positive potential sensors were saturated. This indicates a third event which was capable of very high voltages, but delivered very little current – typically, a benign event.

The negative J-V plots, obtained from die along a row through the center of the wafer, also suggest that their origin was different from the source which gave rise to the negative potentials in Figure 16. The highest negative charging density was recorded on the left side of the wafer, where the sensors saturated at -14V. However, the highest voltage recorded on the J-V plot from that location is - 8V. In the center of the wafer and to the right of it, no response is evident in the negative J-V plots, indicating that the current density was less than $-0.8\mu A/cm^2$. But potentials exceeding -9V were recorded there!



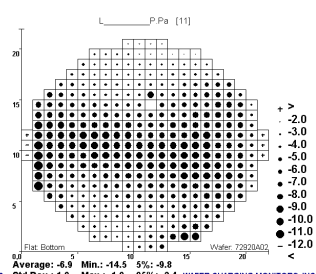


Fig. 15. TEL DRM:
Positive potentials.

Fig. 16. TEL DRM:
Negative potentials.

[4] When a charging event of one polarity is followed by a charging event of the opposite polarity, the SPM technique records the last charging event.

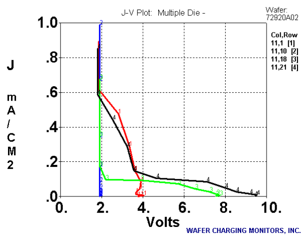


Fig. 17. TEL DRM: Positive J-V.

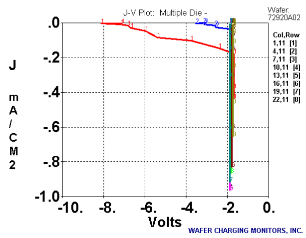


Fig. 18. TEL DRM: Negative J-V.

Additional CHARM-2 experiments, which lead to a detailed understanding of this response, are summarized in M. Kobayashi's paper (a copy of which may also be obtained from Wafer Charging Monitors).

Summary

The preceding examples show that CHARM-2 wafers can provide a rich set of data, which can be "mined" to obtain insights into the charging behavior of plasma process tools. The results are often complex, reflecting the complexity of contemporary tools and processes whose charging behavior cannot be adequately represented by a single wafer map, or a single number – in spite of our wishes. However, even the most complex signatures can be understood by experimenting with subsets of the full process sequence. When the complementary, self-consistent response between the UV map, the potentials maps, and the J-V plots characteristic of a simple plasma is obtained, the culprit is identified – and, typically, that is more than half the battle.

CHARM-2 application procedures

The proper application procedures for different plasma processes are as follows:

• **Resist ashing:** CHARM-2 wafers may be exposed to the ashing plasma for the entire duration of the ashing cycle, just like product wafers. In multi-wafer ashers (such as barrel ashers) position of the wafer in the load is often important!

• **Plasma etching (including ion milling):** Since etching processes remove material from wafers, they can be lethal to CHARM-2 wafers. Metal etching is most dangerous since it can remove the probe pads, making it impossible to read-out the acquired information. Fortunately, the CHARM-2 EEPROM-based sensors respond in less than a millisecond. Therefore, a short exposure to etching plasma is sufficient to capture the charging and UV emissions characteristics of the plasma. To ensure that both the transient and steady-state of the plasma are adequately characterized, the exposure time should be sufficient for the plasma to reach a steady-state. In most cases, a 5 to 10 second exposure is adequate.

• **Oxide deposition:** Since it is essential to remove all deposited oxide from CHARM-2 wafers in order to read-out the acquired information, the deposition cycle should be as short as possible. To ensure that both the transient and steady-state of the plasma are adequately characterized, the deposition time should allow the plasma to reach a steady-state. In most cases, a 5 to 10 second deposition is adequate. The deposited oxide can be removed with plasma or a wet etchant. If it is removed with a plasma, the system used should first be characterized with a CHARM-2 wafer to ensure that the oxide removal process does not cause charging. If the deposited material is removed with a wet etchant, an ammonium-fluoride-buffered HF (BHF) solution should be used, since it is significantly less aggressive toward the Aluminum metalization on CHARM-2 wafers than water-HF solutions. To further reduce the etching of the metalization on CHARM-2 wafers, the overetch time in the BHF solution should be minimized. This can be accomplished by calibrating the BHF etch time using a bare silicon wafer which received the same deposition as the CHARM-2 wafer.

• **Metal deposition:** Since metal deposition will short all probe pads on the CHARM-2 wafer, it is essential to remove the deposited metal from the CHARM-2 wafer in order to read-out the acquired information. To facilitate this, the deposition cycle should be as short as possible. To ensure that both the transient and steady-state of the plasma are adequately characterized, the deposition time should allow the plasma to reach a steady-state. In most cases, a 5 to 10 second deposition is adequate. The deposited metal can be removed with plasma or a wet etchant. If it is removed with a plasma, the system used should first be characterized with a CHARM-2 wafer to ensure that the metal removal process does not cause charging. If the deposited material is removed with a wet etchant, the overetch time in the metal-etch solution should be minimized. This can be accomplished by calibrating the etch time using an oxidized silicon wafer which received the same deposition as the CHARM-2 wafer.

• **Other processes:** Contact WCM for recommendations.

References:

[1] W. Lukaszek, ECS ISTC2001 Proceedings, pp. 606-616.
[2] M-Y Lee, et al, P2ID'99 Proceedings, pp. 104-107.
[3] M. Kobayashi, et al, ECS ISTC2001 Proceedings, pp. 597-605.

HOW TO CONTACT WCM:

If you would like to receive this bulletin or information about our products, services, and publications, or would like to contribute material to this bulletin, please contact:

Wafer Charging Monitors, Inc.
127 Marine Road
Woodside, CA 94062
phone: 650-851-9313
fax: 650-851-2252
web site: www.charm-2.com
email: sales@charm-2.com

